EE/CprE/Se 491 Weekly Report 6
10/18/24 - 10/24/24
sdmay25-28
Digital ASIC fabrication
Client & Advisor: Dr. Duwe

Team Members
Calvin Smith – Issue Tracking
Camden Fergen - Testing Lead
John - Team organizer
Nicholas - Verilog Lead
Levi - Client interaction

Weekly Summary
This week we worked on some project planning and setup as well as setting up the VMs. We all did some research for stuff regarding to efabless. We worked together to build upon the tasks we would be doing and the order of them. We have also worked on getting some code that we can try running on the microcontroller.

Pask Week Accomplishments

- Calvin:
  - installed various software on the VM
  - installed litex on the vm
  - began familiarizing myself with verilator
  - Learned vivado debugging using ILAs during runtime
  - presented 1/5 of a lightning talk without stuttering (big accomplishment)
- Camden:
  - Got into the VM (finally) and started to get software installed
    - Got VScode and a ssh key setup to push files to the repo
    - Installed extensions needed for the VScode verilog stuff
    - Tested pushing/pulling
  - Updated gantt
- John:
  - Helped Nick with datapath one
  - Researched some RISC-V cores
  - Performed research for the main differences between MIPS and RISC-V
- Levi:
  - Worked on presentations

- Nicholas:
    - Wrote tests for datapath one.
    - Fixed some issues with datapath one.
    - Researched and wrote code for MCU in C for datapath one.

Name	Individual Contribution	Hours this Week	Hours Cumulative
Calvin	-VM installations -Debian-based knowledge -fpga debugging research -good vibes -Provided Dr. Duwe with much needed hair	7.121	36.044
Camden	Still working ont he VMS, ETG has been helping but slowing me down. Getting the final stuff installed. Updated gantt chart	6	36
John	-Helped Nick with datapath one -Researched some RISC-V cores -Performed research for the main differences between MIPS and RISC-V	6	36
Levi	Created Graphics	6	36
Nicholas	Datapath one testing and coding	6	40

<u>Plans for Upcoming Week</u>

- Calvin:
  - continue with hardware testing on FPGAs
  - understand how to create an interface on the zedboards for hardware testing
  - convert a litex core to a pure verilog project we can simulate
  - be an upstanding gentleman
- Camden:

    - Finish the VM setup and get it cloned. Try programming MCU and write some test code for it to know how it works (sorta).
    - Update more gantt!
- John:
    - Work with Nick to test datapath one and program it onto to microcontroller
    - Play around with the microcontroller and caravel
    - More research on RISC-V cores and design
- Levi:
    - Research software or QOL stuff to add to VM (VIMRCs etc.)
- Nicholas:
    - Fully test datapath one.
    - Test programming the MCU.

Summary of weekly advisor meeting

During our advisor meeting, we talked to Duwe about our questions regarding CGRAs and gave our ideas for possible applications. He mentioned that we should try focusing more on getting our basic stuff to work (i.e., get our RISC-V processor on the board before worrying about our CGRA or accelerator). He mentioned that we should work on getting code running on the microcontroller.